

WHAT IS CLAIMED IS:

1 1. A demodulator for demodulating a set of S possible
2 orthogonal modulation codes received serially as binary data,
3 wherein each of said orthogonal modulation codes comprises M binary
4 bits representing an N-bit data symbol and wherein $M = 2^N$, said
5 demodulator comprising:

6 a Logic 00 input detector capable of comparing sequential
7 pairs of said M binary bits of said serially received orthogonal
8 modulation codes to a Logic 00 value and outputting a [+1,+1]
9 signal if a match occurs and outputting a [-1,-1] signal if a match
10 does not occur;

11 a summation circuit comprising S accumulators;

12 a Logic 00 switch array comprising S switches, wherein a
13 Kth one of said S switches in said Logic 00 switch array is capable
14 of coupling an output of said Logic 00 input detector to a first
15 input of a Kth one of said S accumulators;

16 a storage array capable of storing S code masks
17 associated with said S orthogonal modulation codes, wherein each of
18 said S code masks comprises M/2 code mask bits and each of said M/2
19 code mask bits is associated with a corresponding one of said
20 sequential pairs of said M binary bits in one of said orthogonal
21 modulation codes; and

22 control circuitry capable of synchronously applying the
23 M/2 code mask bits in a Kth one of said S code masks in said

24 storage array as a switch control signal to said Kth switch in said
25 Logic 00 switch array such that a Logic 1 code mask bit in said Kth
26 code mask closes said Kth switch in said Logic 00 switch array
27 whenever said Logic 00 input detector is comparing a sequential
28 pair of said M binary bits equal to 00, thereby connecting the
29 [+1,+1] output signals of said Logic 00 input detector to said
30 first input of said Kth accumulator.

1 2. The demodulator as set forth in Claim 1 further
2 comprising:

3 a Logic 01 input detector capable of comparing sequential
4 pairs of said M binary bits of said serially received orthogonal
5 modulation codes to a Logic 01 value and outputting a [+1,+1]
6 signal if a match occurs and outputting a [-1,-1] signal if a match
7 does not occur; and

8 a Logic 01 switch array comprising S switches, wherein a
9 Kth one of said S switches in said Logic 01 switch array is capable
10 of coupling an output of said Logic 01 input detector to a second
11 input of said Kth accumulator, wherein said control circuitry is
12 capable of synchronously applying the M/2 code mask bits in said
13 Kth code mask in said storage array as a switch control signal to
14 said Kth switch in said Logic 01 switch array such that a Logic 1
15 code mask bit in said Kth code mask closes said Kth switch in said
16 Logic 01 switch array whenever said Logic 01 input detector is
17 comparing a sequential pair of said M binary bits equal to 01,
18 thereby connecting the [+1,+1] output signals of said Logic 01
19 input detector to said second input of said Kth accumulator.

1 3. The demodulator as set forth in Claim 2 further
2 comprising:

3 a Logic 10 input detector capable of comparing sequential
4 pairs of said M binary bits of said serially received orthogonal
5 modulation codes to a Logic 10 value and outputting a [+1,+1]
6 signal if a match occurs and outputting a [-1,-1] signal if a match
7 does not occur; and

8 a Logic 10 switch array comprising S switches, wherein a
9 Kth one of said S switches in said Logic 10 switch array is capable
10 of coupling an output of said Logic 10 input detector to a third
11 input of said Kth accumulator, wherein said control circuitry is
12 capable of synchronously applying the M/2 code mask bits in said
13 Kth code mask in said storage array as a switch control signal to
14 said Kth switch in said Logic 10 switch array such that a Logic 1
15 code mask bit in said Kth code mask closes said Kth switch in said
16 Logic 10 switch array whenever said Logic 10 input detector is
17 comparing a sequential pair of said M binary bits equal to 10,
18 thereby connecting the [+1,+1] output signals of said Logic 10
19 input detector to said third input of said Kth accumulator.

1 4. The demodulator as set forth in Claim 3 further
2 comprising:

3 a Logic 11 input detector capable of comparing sequential
4 pairs of said M binary bits of said serially received orthogonal
5 modulation codes to a Logic 11 value and outputting a [+1,+1]
6 signal if a match occurs and outputting a [-1,-1] signal if a match
7 does not occur; and

8 a Logic 11 switch array comprising S switches, wherein a
9 Kth one of said S switches in said Logic 11 switch array is capable
10 of coupling an output of said Logic 11 input detector to a fourth
11 input of said Kth accumulator, wherein said control circuitry is
12 capable of synchronously applying the M/2 code mask bits in said
13 Kth code mask in said storage array as a switch control signal to
14 said Kth switch in said Logic 11 switch array such that a Logic 1
15 code mask bit in said Kth code mask closes said Kth switch in said
16 Logic 11 switch array whenever said Logic 11 input detector is
17 comparing a sequential pair of said M binary bits equal to 11,
18 thereby connecting the [+1,+1] output signals of said Logic 11
19 input detector to said fourth input of said Kth accumulator.

1 5. The demodulator as set forth in Claim 4 further
2 comprising a code selection circuit capable of reading a sum value
3 from each said S accumulators and identifying an accumulator
4 containing a maximum sum value.

1 6. The demodulator as set forth in Claim 5 wherein said code
2 selection circuit outputs one of 2^M N-bit data symbols
3 corresponding to said identified accumulator containing said
4 maximum value.

1 7. The demodulator as set forth in Claim 6 wherein $N = 6$ and
2 $M = 2^N = 64$.

1 8. The demodulator as set forth in Claim 7 wherein $S = 64$.

1 9. The demodulator as set forth in Claim 8 wherein said
2 orthogonal modulation codes are Walsh codes.

1 10. A code division multiple access (CDMA) wireless network
2 comprising a plurality of base transceiver stations capable of
3 communicating with access terminals located in a coverage area of
4 said wireless network, wherein a first one of said plurality of
5 base transceiver stations comprises:

6 a demodulator for demodulating a set of S possible
7 orthogonal modulation codes received serially as binary data,
8 wherein each of said orthogonal modulation codes comprises M binary
9 bits representing an N-bit data symbol and wherein $M = 2^N$, said
10 demodulator comprising:

11 a Logic 00 input detector capable of comparing
12 sequential pairs of said M binary bits of said serially
13 received orthogonal modulation codes to a Logic 00 value and
14 outputting a [+1,+1] signal if a match occurs and outputting
15 a [-1,-1] signal if a match does not occur;

16 a summation circuit comprising S accumulators;

17 a Logic 00 switch array comprising S switches,
18 wherein a Kth one of said S switches in said Logic 00 switch
19 array is capable of coupling an output of said Logic 00 input
20 detector to a first input of a Kth one of said S accumulators;

21 a storage array capable of storing S code masks
22 associated with said S orthogonal modulation codes, wherein
23 each of said S code masks comprises M/2 code mask bits and
24 each of said M/2 code mask bits is associated with a

25 corresponding one of said sequential pairs of said M binary
26 bits in one of said orthogonal modulation codes; and

27 control circuitry capable of synchronously applying
28 the M/2 code mask bits in a Kth one of said S code masks in
29 said storage array as a switch control signal to said Kth
30 switch in said Logic 00 switch array such that a Logic 1 code
31 mask bit in said Kth code mask closes said Kth switch in said
32 Logic 00 switch array whenever said Logic 00 input detector is
33 comparing a sequential pair of said M binary bits equal to 00,
34 thereby connecting the [+1,+1] output signals of said Logic 00
35 input detector to said first input of said Kth accumulator

1 11. The CDMA wireless network as set forth in Claim 10
2 further comprising:

3 a Logic 01 input detector capable of comparing sequential
4 pairs of said M binary bits of said serially received orthogonal
5 modulation codes to a Logic 01 value and outputting a [+1,+1]
6 signal if a match occurs and outputting a [-1,-1] signal if a match
7 does not occur; and

8 a Logic 01 switch array comprising S switches, wherein a
9 Kth one of said S switches in said Logic 01 switch array is capable
10 of coupling an output of said Logic 01 input detector to a second
11 input of said Kth accumulator, wherein said control circuitry is
12 capable of synchronously applying the M/2 code mask bits in said
13 Kth code mask in said storage array as a switch control signal to
14 said Kth switch in said Logic 01 switch array such that a Logic 1
15 code mask bit in said Kth code mask closes said Kth switch in said
16 Logic 01 switch array whenever said Logic 01 input detector is
17 comparing a sequential pair of said M binary bits equal to 01,
18 thereby connecting the [+1,+1] output signals of said Logic 01
19 input detector to said second input of said Kth accumulator.

1 12. The CDMA wireless network as set forth in Claim 11
2 further comprising:

3 a Logic 10 input detector capable of comparing sequential
4 pairs of said M binary bits of said serially received orthogonal
5 modulation codes to a Logic 10 value and outputting a [+1,+1]
6 signal if a match occurs and outputting a [-1,-1] signal if a match
7 does not occur; and

8 a Logic 10 switch array comprising S switches,
9 wherein a Kth one of said S switches in said Logic 10 switch array
10 is capable of coupling an output of said Logic 10 input detector to
11 a third input of said Kth accumulator, wherein said control
12 circuitry is capable of synchronously applying the M/2 code mask
13 bits in said Kth code mask in said storage array as a switch
14 control signal to said Kth switch in said Logic 10 switch array
15 such that a Logic 1 code mask bit in said Kth code mask closes said
16 Kth switch in said Logic 10 switch array whenever said Logic 10
17 input detector is comparing a sequential pair of said M binary bits
18 equal to 10, thereby connecting the [+1,+1] output signals of said
19 Logic 10 input detector to said third input of said Kth
20 accumulator.

1 13. The CDMA wireless network as set forth in Claim 12
2 further comprising:

3 a Logic 11 input detector capable of comparing sequential
4 pairs of said M binary bits of said serially received orthogonal
5 modulation codes to a Logic 11 value and outputting a [+1,+1]
6 signal if a match occurs and outputting a [-1,-1] signal if a match
7 does not occur; and

8 a Logic 11 switch array comprising S switches, wherein a
9 Kth one of said S switches in said Logic 11 switch array is capable
10 of coupling an output of said Logic 11 input detector to a fourth
11 input of said Kth accumulator, wherein said control circuitry is
12 capable of synchronously applying the M/2 code mask bits in said
13 Kth code mask in said storage array as a switch control signal to
14 said Kth switch in said Logic 11 switch array such that a Logic 1
15 code mask bit in said Kth code mask closes said Kth switch in said
16 Logic 11 switch array whenever said Logic 11 input detector is
17 comparing a sequential pair of said M binary bits equal to 11,
18 thereby connecting the [+1,+1] output signals of said Logic 11
19 input detector to said fourth input of said Kth accumulator.

1 14. The CDMA wireless network as set forth in Claim 13
2 further comprising a code selection circuit capable of reading a
3 sum value from each said S accumulators and identifying an
4 accumulator containing a maximum sum value.

1 15. The CDMA wireless network as set forth in Claim 14
2 wherein said code selection circuit outputs one of 2^M N-bit data
symbols corresponding to said identified accumulator containing
said maximum value.

1 16. The CDMA wireless network as set forth in Claim 15
2 wherein $N = 6$ and $M = 2^N = 64$.

1 17. The CDMA wireless network as set forth in Claim 16
2 wherein $S = 64$.

1 18. The CDMA wireless network as set forth in Claim 17
2 wherein said orthogonal modulation codes are Walsh codes.

1 19. For use in a base station of a wireless network capable
2 of communicating with mobile stations located in a coverage area of
3 the wireless network, a method of demodulating a set of S possible
4 orthogonal modulation codes received serially as binary data,
5 wherein each of the orthogonal modulation codes comprises M binary
6 bits representing an N-bit data symbol and wherein $M = 2^N$, the
7 method comprising the steps of:

 in a Logic 00 input detector, comparing sequential pairs
of the M binary bits of the serially received orthogonal modulation
codes to a Logic 00 value and outputting a [+1,+1] signal if a
match occurs and outputting a [-1,-1] signal if a match does not
occur;

 retrieving from a storage array the Kth one of S code
masks associated with the S orthogonal modulation codes, wherein
each of the S code masks comprises M/2 code mask bits and each of
the M/2 code mask bits is associated with a corresponding one of
the sequential pairs of the M binary bits in one of the orthogonal
modulation codes; and

 synchronously applying the M/2 code mask bits of the Kth
S code mask as a switch control signal to the Kth switch in a
Logic 00 switch array comprising S switches, wherein the Kth switch
in the Logic 00 switch array is capable of coupling an output of
the Logic 00 input detector to a first input of a Kth one of S
accumulators, and wherein a Logic 1 code mask bit in the Kth code

1 20. The method as set forth in Claim 19 further comprising
2 the steps of:

3 in a Logic 01 input detector, comparing sequential pairs
4 of the M binary bits of the serially received orthogonal modulation
5 codes to a Logic 01 value and outputting a [+1,+1] signal if a
6 match occurs and outputting a [-1,-1] signal if a match does not
7 occur; and

8 synchronously applying the M/2 code mask bits of the Kth
9 S code mask as a switch control signal to the Kth switch in a
10 Logic 01 switch array comprising S switches, wherein the Kth switch
11 in the Logic 01 switch array is capable of coupling an output of
12 the Logic 01 input detector to a second input of the Kth
13 accumulator, and wherein a Logic 1 code mask bit in the Kth code
14 mask closes the Kth switch in the Logic 01 switch array whenever
15 the Logic 01 input detector is comparing a sequential pair of the
16 M binary bits equal to 01, thereby connecting the [+1,+1] output
17 signals of the Logic 01 input detector to the second input of the
18 Kth accumulator.

1 21. The method as set forth in Claim 20 further comprising
2 the steps of:

3 in a Logic 10 input detector, comparing sequential pairs
4 of the M binary bits of the serially received orthogonal modulation
5 codes to a Logic 10 value and outputting a [+1,+1] signal if a
6 match occurs and outputting a [-1,-1] signal if a match does not
7 occur; and

8 synchronously applying the M/2 code mask bits of the Kth
9 S code mask as a switch control signal to the Kth switch in a
10 Logic 10 switch array comprising S switches, wherein the Kth switch
11 in the Logic 10 switch array is capable of coupling an output of
12 the Logic 10 input detector to a third input of the Kth
13 accumulator, and wherein a Logic 1 code mask bit in the Kth code
14 mask closes the Kth switch in the Logic 10 switch array whenever
15 the Logic 10 input detector is comparing a sequential pair of the
16 M binary bits equal to 10, thereby connecting the [+1,+1] output
17 signals of the Logic 10 input detector to the third input of the
18 Kth accumulator.

1 22. The method as set forth in Claim 21 further comprising
2 the steps of:

3 in a Logic 11 input detector, comparing sequential pairs
4 of the M binary bits of the serially received orthogonal modulation
5 codes to a Logic 11 value and outputting a [+1,+1] signal if a
6 match occurs and outputting a [-1,-1] signal if a match does not
7 occur; and

8 synchronously applying the M/2 code mask bits of the Kth
9 S code mask as a switch control signal to the Kth switch in a
10 Logic 11 switch array comprising S switches, wherein the Kth switch
11 in the Logic 11 switch array is capable of coupling an output of
12 the Logic 11 input detector to a fourth input of the Kth
13 accumulator, and wherein a Logic 1 code mask bit in the Kth code
14 mask closes the Kth switch in the Logic 11 switch array whenever
15 the Logic 11 input detector is comparing a sequential pair of the
16 M binary bits equal to 11, thereby connecting the [+1,+1] output
17 signals of the Logic 11 input detector to the fourth input of the
18 Kth accumulator.